40GBase QSFP+ Parallel LR4 1.5km

Optical Transceivers with isolators

Features:

- Supports 41.2 Gb/s aggregate bit rates
- Link Distance up to 1.5km over SMF fiber
- 4 parallel 10Gbps full duplex channels
- Standard 12-fiber MPO/MTP APC SMF connector
- Compatible with 4 SFP+ 10GBASE LR / LR lite transceivers via SMF breakout cable
- Uncooled 4x10Gb/s transmitter/PIN Diode with isolators
- Power dissipation < 2.5W
- Compliant with Hot Pluggable QSFP+ MSA (SFF-8436)
- Digital Diagnostic Monitoring Interface
- Operating case temperature range: 0°C~70°C
- RoHS 6 Compliant

Applications:

- 40GBASE IEEE Interconnect up to 1.5km over SMF fiber
- High Performance, High Density Interconnect
- Data center Rack-Rack, Rack to cluster interconnect

Absolute Maximum Ratings

Parameter	Symbol	Unit	Min	Max
Storage Temperature Range	T_s	°C	-40	+85
Power Supply Voltage	V_{cc}	V	0	+3.6
Relative Humidity	RH	%	5	85

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Recommended Operating Conditions

Parameter	Symbol	Unit	Min	Typ	Max
Case Operating Temperature Range	T_{c-CT}	°C	0	25	+70
Power Supply Voltage	V_{cc}	V	3.135	3.3	3.465
Power Supply Current	I_{cc}	mA			721
Power Consumption		W			2.5
Data rate per Channel		Gbps		10.3125	

Specifications (tested under recommended operating conditions, unless otherwise noted)

Parameter	Symbol	Unit	Min.	Typ.	Max.	Notes
Electrical Characteristics						
Transmitter Differential Input Voltage	V_{IN}	mV_{pp}	180		800	
Receiver Differential Output Voltage	V_O	mV_{pp}	400	450	850	1
Loss of Signal (LOS)	V_{OH}	V	2		Vcc	2
	V_{OL}		Vee		Vee+0.8	
Transmitter Disable (TX-Disable)	V_{IH}	V	2		Vcc	
	V_{IL}		Vee		Vee+0.8	
Rx Output Rise and Fall Time	Tr/Tf	ps	28			20% to 80%

Note1. SFF-8431, SFP+MODULE RECEIVER OUTPUT SPECIFICATIONS AT C'.

Note2. LOS is an open collector output. Should be pulled up with 4.7kΩ – 10kΩ on the host board. Normal operation is logic 0; loss of signal is logic 1.

Optical transmitter Characteristics						
Parameter	**Symbol**	**Unit**	**Min.**	**Typ.**	**Max.**	**Notes**
Average Launch Power, each lane	Po	dBm	-8.2		+0.5	
Center wavelength	λ_c	nm	1260		1355	
Optical Spectral Width (RMS)	$\Delta\lambda$	nm			3.5	Target 2.5
Extinction ratio	E_R	Db	3.5			
Optical power OMA, each lane	P_{OMA}	dBm	-4.5		+1.5	1
Launch power in OMA minus TDP, each lane	O-T	dB	-9.4			
Average launch power of OFF transmitted, each lane	P_{off}	dBm			-30	

$RIN_{12}OMA$	RIN	dB/Hz			-128	
Optical return loss tolerance	ORL_T	dB	12			2
Output eye	Compliant with IEEE802.3ba eye mask					
Optical receiver Characteristics						
Parameter	**Symbol**	**Unit**	**Min.**	**Typ.**	**Max.**	**Notes**
Center Wavelength	λ_c	nm	1260		1355	
Receiver Overload in OMA, each lane	Rx_{OMA}	dBm	+1.5			
Receiver Overload in average power, each lane	P_{max}	dBm	+0.5			3
Average receive power, each lane	RxPx	dBm	-12.5			4
Receiver Sensitivity in OMA, each lane	Sen_{OMA}	dBm			-11.5	5
Receiver Crossing	R_{CP}	%	45		55	
Receiver Eye Mask	SFF-8431, SFP+MODULE RECEIVER OUTPUT SPECIFICATIONS AT C'.					
Receiver Eye Mask Margin	R_{EMM}	%	0			
Receiver Reflectance	R_{rx}	dB			-12	
LOS Assert	LOS_A	dBm	-30			
LOS Deassert	LOS_D	dBm			-12	
LOS Hysteresis	LOS_H	dB	0.5		6	

Notes:

1. Even if the TDP < 1 dB, the OMA (min) must exceed this value
2. Transmitter reflectance is defined looking into the transmitter
3. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having a power level equal to the average receive power (max) plus at least 1 dB.
4. Average receive power (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. PRBS 231-1 at BER 10-12, ER=3.5dB

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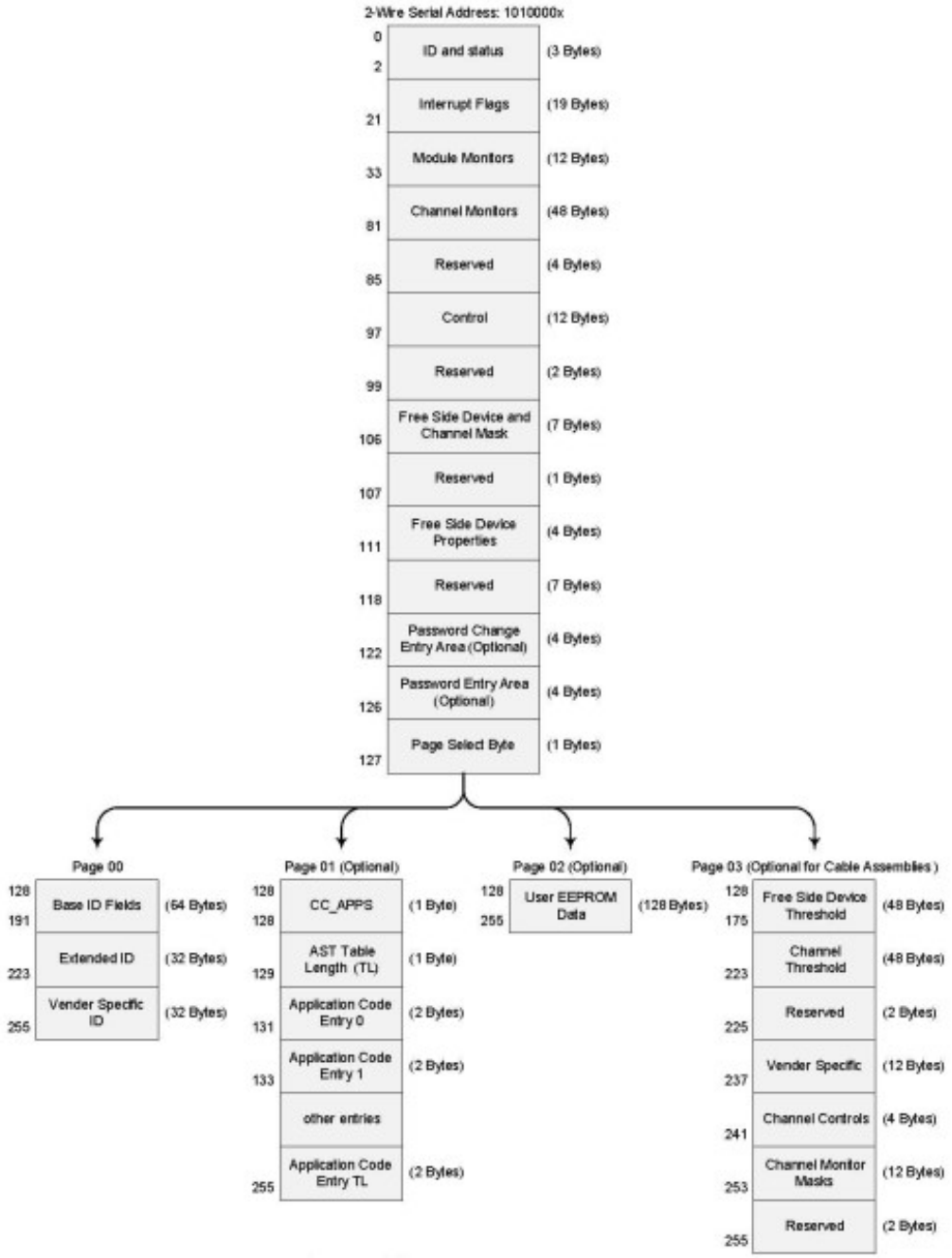
Digital Diagnostic Memory Map



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EEPROM Serial ID Memory Contents

Accessing Serial ID Memory uses the 2 wire address 1010000X (A0H). Memory Contents of Serial ID are shown in Table as below.

Serial ID Memory Contents

Data Address	Size (Bytes)	Name of Field	Contents(Hex)	Description
BASE ID FIELDS				
0	1	Identifier	0D	QSFP
1-2	2	Status Indicator	00 00	
3-21	19	Interrupt Flags	All 00	
22-33	12	Module Monitors	All 00	
34-81	48	Channel Monitors	All 00	
82-85	4	Reserved	00 00 00 00	
86-97	12	Control	All 00	
98-99	2	Reserved	00 00	
100-106	7	Module & Channel Masks	00 00 00 00 00 00 00	
107-118	12	Reserved	All 00	
119-122	4	Password Change Entry	00 00 00 00	
123-126	4	Password Entry	00 00 00 00	
127	1	Page Select	00	
128	1	Identifier	0D	QSFP+
129	1	Ext. Identifier	80	
130	1	Connector	0C	MPO Connector
131-138	8	Specification Compliance	80 00 00 00 00 00 00 00	40G PSM4 over 1.5km
139	1	Encoding	05	64B/66B
140	1	BR-Normal	67	10.3Gbps per lane
141	1	Extended Rate Select	00	unspecified
142	1	Length SM-km	01	1.5km SMF
143	1	Length, OM3-2m	00	
144	1	Length, OM2-1m	00	
145	1	Length, OM1-1m	00	
146	1	Length, Cu-1m	00	not support copper
147	1	Device technology	30	1310nm FP

148-163	16	Vendor name	57 41 56 45 53 50 4C 49 54 54 45 52 20 20 20 20	EGISMOS
164	1	Extended Module Codes	00	
165-167	3	Vendor OUI	00 0F 0E	
168-183	16	Vendor Part Number	57 53 54 2D 51 53 46 50 2B 50 4C 34 4C 2D 43 20	EGS-QSFP+PL4L-C
184-185	2	Vendor rev	31 30	10
186-187	2	Wavelength	66 58	1310nm
188-189	2	Wavelength Tolerance	27 10	50nm
190	1	Max case temp	46	70C
191	1	Check code for [128-190]	Xx	
192-195	4	Options	12 00 00 00	40G PSM4 parallel SM
196-211	16	Vendor SN	CC CM YY MM ID SN SN SN SN 20 20 20 20 20 20 20	CC: Country code CM: CM code YY: Year MM: Month ID: Product ID SN: Sequence
212-219	8	Date code	YY YY MM MM DD DD LL LL	YY: Year MM: Month DD: Day of month LL: Lot number
220	1	DOM type	08	For average power
221	1	Enhanced Options	00	
222	1	Reserved	00	
223-255	33	Vendor specified	Xx	

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Low Speed Electrical Specification

Low Speed Control and Sense Signals

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3.0mA
	VOH	Vcc-0.5	Vcc+0.3	V	
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O pin	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	3.0 k Ohms Pullup resistor, max
			200	pF	1.6 k Ohms pullup resistor max
LPMode, Reset and ModSelL	VIL	-0.3	0.8	V	|Iin|<=125 uA for 0V<Vin,Vcc
	VIH	2	VCC+0.3	V	
ModPrsL and IntL	VOL	0	0.4	V	IOL=2.0mA
	VOH	VCC-0.5	VCC+0.3	V	

Pin Definition

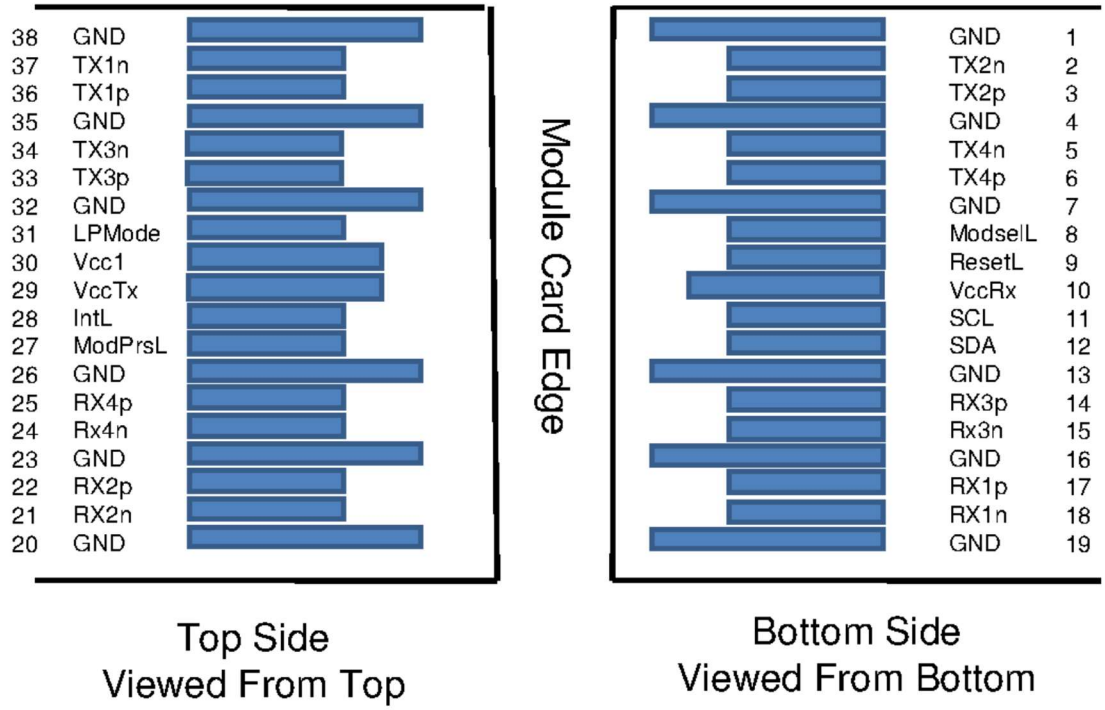

Figure 1: Interface to Host PCB

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Module Electrical Pin Definition

Pin Function Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

Note 1: GND is the symbol for signal and supply (power) common for the QSFP+ module. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 6. Recommended host board power supply filtering is shown in Figures 3 and 4. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP+ Module in any combination. The connector pins are each rated for a maximum current of 500 mA.

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Application in System

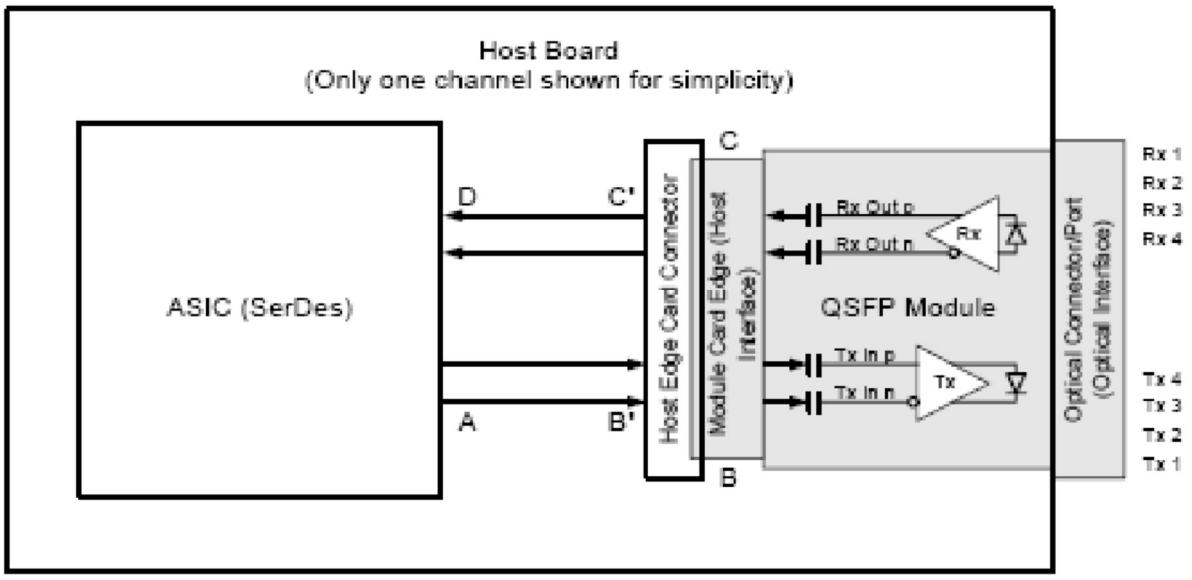

Figure 2: Application Reference Model

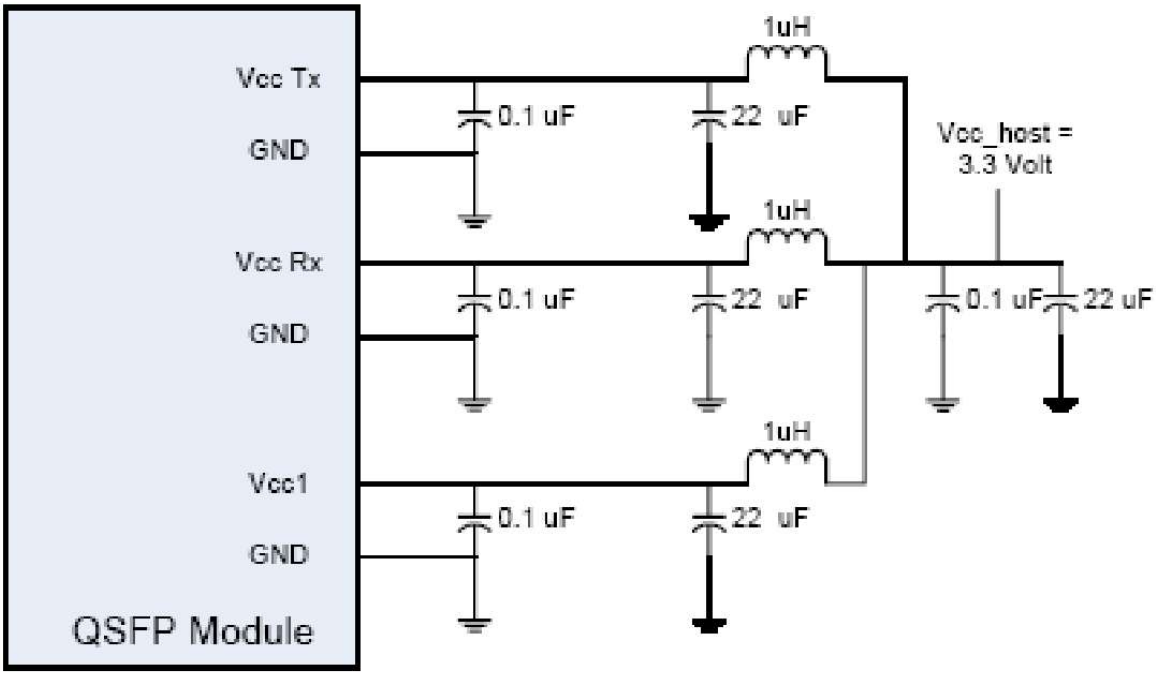

Figure 3: Recommended Host Board Power Supply Filtering

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Typical Application Circuit

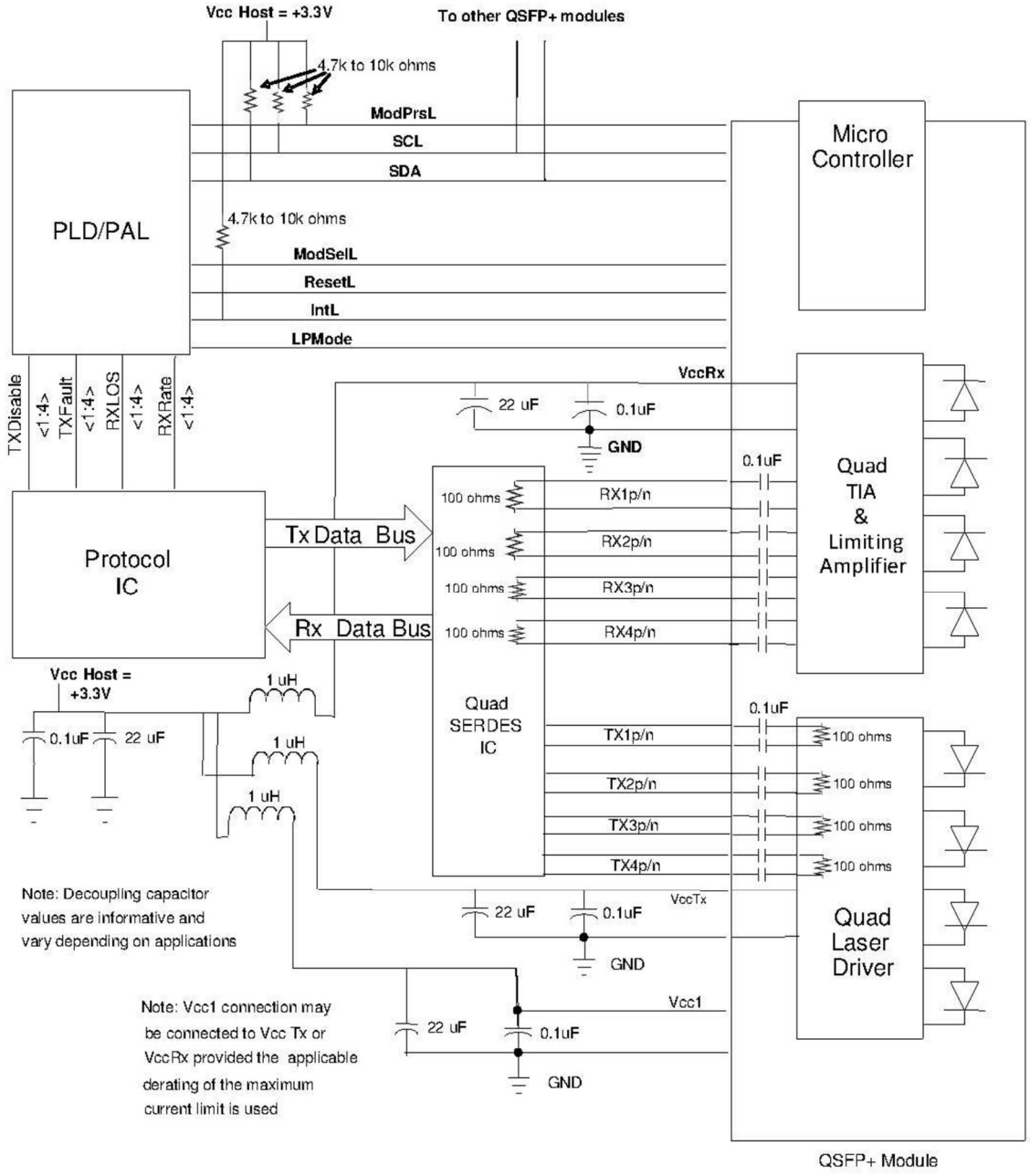

Figure 4: Example QSFP+ Host Board Schematic for Optical Modules

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Mechanical

Comply to SFF-8436 rev. 4.2, for QSFP+ 10 Gbs 4X PLUGGABLE TRANSCEIVER, tab color in yellow

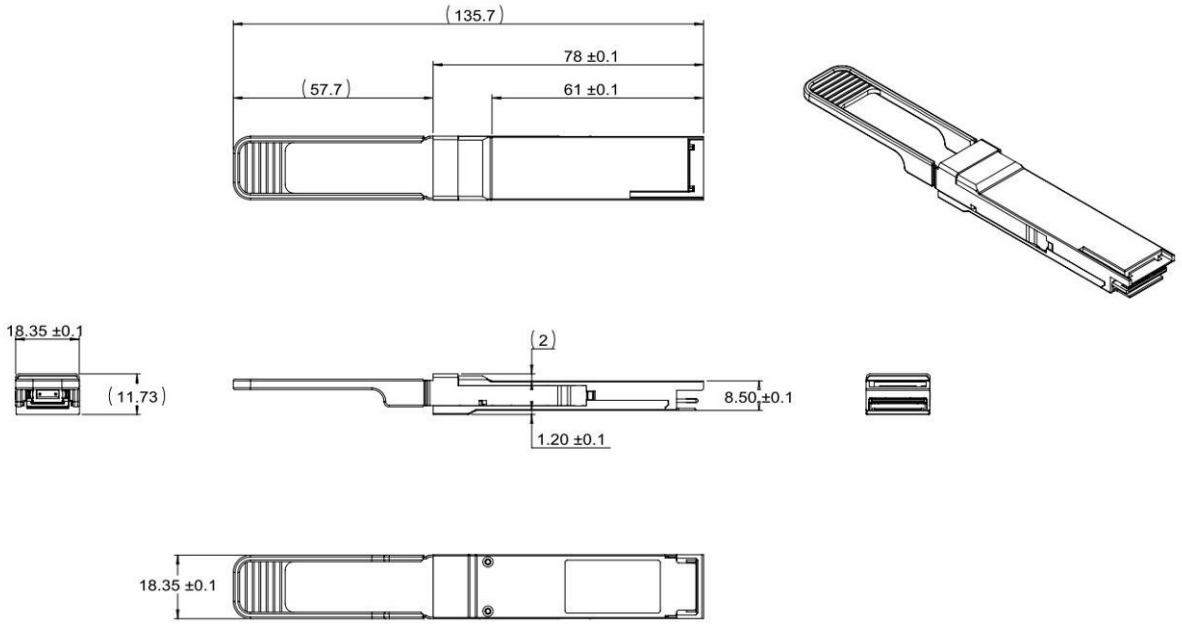

Figure 5: Drawing of QSFP+ Module

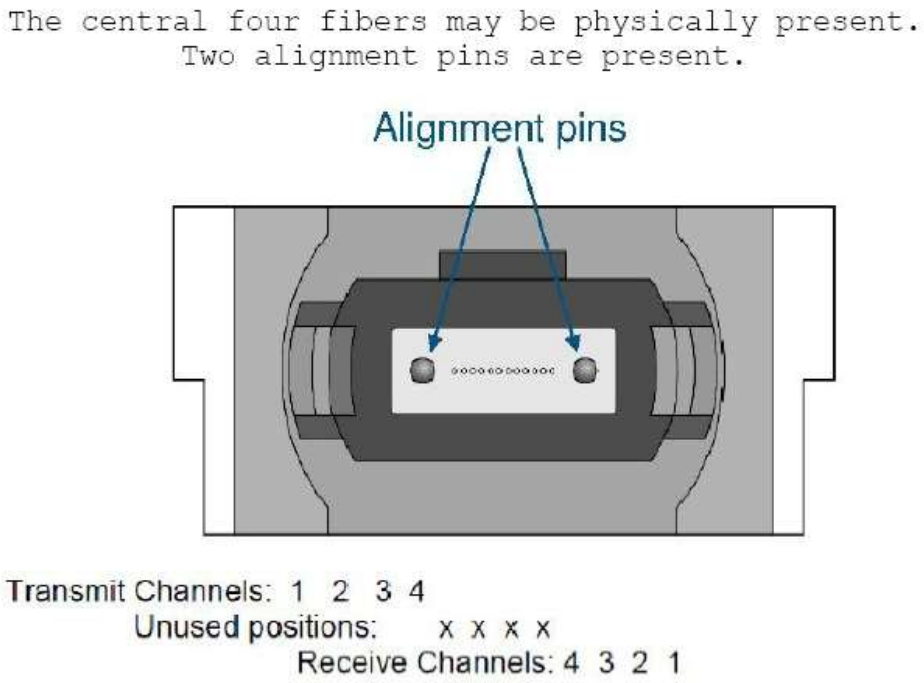

Figure 6: QSFP+ Optical Receptacle and Channel Orientation for MPO/APC connector

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Regulatory Compliance

Feature	Test Method	Performance
Laser Eye Safety	FDA 21 CFR 1040.10 and 1040.11 IEC 60825-1: 1994+ A11: 1996+ A2: 2001 IEC 60825-2: 2004 + A1: 2006 EN 60825-1:1994+A1:2002+A2:2001 EN 60825-2: 2004	Compliant with Class 1 laser product
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.4 Human Body Model	Class 1 (>1.5kV)
Electrostatic Discharge (ESD) Immunity	IEC 61000-4-2: 2001	Class 2 (>4.0kV)
Electromagnetic Interference (EMI)	FCC Part 15 Subpart J Class B CISPR22:1997+A1:2000+A2:2002, Class B EN55022:1998+A1:2000+A2:2003, Class B	Compliant with standards

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Sum Up

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power	Detector	Max. Receive Sensitivity	Temp	Reach	Other	Application code
EGS-QSFP+PL4L-C	QSFP+	10.3 Gbps	1310nm FP with isolators	-8.2 dBm~ +0.5 dBm	PIN	-11.5 dBm in OMA	0~70°C	1.5km for SMF	DDM RoHS	40GBASE-PSM4

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